coupled to a first vertical select gate and a last NROM memory cell of each NAND architecture memory string is coupled to a second vertical select gate.

[0019] For another embodiment, the invention provides a method of forming a NAND architecture memory cell string comprising forming one or more raised areas on a substrate, the raised areas defining associated intervening trenches. The method further includes forming a plurality of NROM memory cells on the sidewalls of the one or more raised areas, forming one or more source/drain regions on the top of the one or more raised areas and at the bottom of the one or more associated intervening trenches, and forming a first vertical select gate coupled to a first NROM memory cell of the string and a second vertical select gate coupled to a last NROM memory cell of the string.

[0020] Other embodiments are also described and claimed.

Brief Description of the Drawings

[0021] Figure 1 shows a cross-sectional view of a typical prior art NROM cell.

[0022] Figure 2 shows a cross-sectional view of a typical prior art NROM cell with a channel less than 100 nm.

[0023] Figures 3A and 3B detail erase operations in NROM memory cells.

[0024] Figures 4A-4C detail a planar NAND NROM memory array of the prior art.

[0025] Figures 5A-5C detail a planar NOR NROM memory array of the prior art.

[0026] Figures 6A-6C detail vertical NOR NROM memory array and cells in accordance with embodiments of the present invention.

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[0027] Figures 7A and 7B detail vertical NAND NROM memory array and cells in accordance with embodiments of the present invention.

[0028] Figures 8A-8C detail formation of a vertical NAND architecture NROM memory array having NROM memory cells and select gates in accordance with embodiments of the present invention.